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Optical link based readout system for Medipix2 quad X-ray detector

V. Fanti[a], R. Marzeddu[a,*], P. Randaccio[a], A. Aloisio[c], A. Del Guerra[d], N. Lanconelli[b], G. Mettivier[c], M.C. Montesi[c], R. Pani[e], P. Russo[c]

[a]*Università di Cagliari e INFN Sez. Cagliari, S.P. Monserrato-Sestu km. 0.7, 09042 Monserrato (CA), Italy*
[b]*Università di Bologna e INFN Sez. Bologna, viale C. Berti Pichat 6/7, 40127 Bologna (BO), Italy*
[c]*Università di Napoli "Federico II" e INFN Sez. Napoli, via Cinthia, 80126 Napoli (NA), Italy*
[d]*Università di Pisa e INFN Sez. Pisa, largo B. Pontecorvo 3, 56127 Pisa (PI), Italy*
[e]*Università di Roma "La Sapienza", viale Regina Elena 324, 00161 Roma (RO), Italy*

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Abstract

An imaging system based on the Medipix2, a single photon counting pixel readout ASIC for X-ray hybrid detectors, has been developed for tomography imaging applications. The "quad assembly" houses four Medipix2 chips placed in a 2×2 array with an active area of about $3 \times 3\,cm^2$. The readout system we present consists of four electronic cards and exploits the Medipix2 parallel readout mode and a fast optical link based on the Glink standard, giving high flexibility and EM interference immunity over long distance connections. A PCI board interfaces the imaging system to a standard PC. We expect a frame rate of 25 frame/s which allows real-time X-ray imaging acquisitions and fast computed tomography (CT) scanning. In this paper, we describe the DAQ project and the status of development.

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Keywords: X-ray imaging; Data acquisition; PCI interface; Optical link

1. Introduction

The Pixel Detector with Optical Parallel Readout for Computed Tomography (PPC) project, funded by the Italian National Institute for Nuclear Physics (INFN) aims to investigate the computed tomography (CT) technique with direct conversion pixel detectors in the field of small animal research field with direct conversion pixel detectors. In this framework, we have designed a dedicated data acquisition system (DAQ) based on the single-photon counting Medipix2 detector developed at CERN in the framework of the Medipix Collaboration [1].

The readout system we present consists of four electronic cards and a host PC. It features a fast optical link to connect the host PC to the detector stage and an acquisition rate up to 25 frame/s, suitable for dynamic X-ray imaging or CT scanning.

2. The Medipix2 detector

Medipix2 [2] is a pixel readout ASIC for hybrid X-ray detectors. It consists of a 256×256 pixel array with 55 μm pitch: each pixel houses the analog and digital electronics to detect, count and store the pulses derived from the photon interaction within the sensor layer. The 13 bit deep counter works in pseudorandom mode so it can store up to 8000 events; a 14th bit signals the overflow condition.

The Medipix2 works in single-photon counting mode so that each incoming photon having an energy above a tunable threshold (single mode) or between two thresholds (window mode) is counted. Moreover, it exploits the so called hybrid architecture: the same readout chip can be coupled by bump bonding with different semiconductor sensors so that different sensor layers can be used, depending on the specific application requirements.

Two modalities are provided for the chip readout: *serial*, through one LVDS[1] data line, or *parallel*, through a 32-bit

*Corresponding author. Tel.: +39 070 675 4967; fax: +39 070 510 212.
E-mail address: roberto.marzeddu@ca.infn.it (R. Marzeddu).

[1]LVDS stands for Low Voltage Differential Signaling.

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wide CMOS[2] bus. Both solutions have been successfully tested by different members of the Medipix collaboration [3–8].

The *quad* Medipix2 assembly consists of four single chips placed on a 2×2 matrix covering a $2.8 \times 2.8\,cm^2$ active area.

3. The system architecture

3.1. Preliminary design considerations

The aim of this project is the development of a readout system based on the Medipix2 quad detector, with an optical interconnection between the detector and the host PC: the available acquisition rate must be 25 frame/s. These features are primarily tailored toward small-animal CT application but real time 2-D radiography studies can also be successfully accomplished. Taking into account that the Medipix2 matrix is about 1 Mbit in size (256×256 pixels each with a 14-bit deep counter) and that each frame takes 40 ms to be read and considering a 10% maximum latency (or dead-time) for data readout and acquisition, a simple computation shows that for each image 458,752 bytes have to be acquired in 4 ms, corresponding to a 115 Mbyte/s throughput. Exploiting the Medipix2 parallel readout mode, this means that the minimum readout frequency must be about 30 MHz. Note that using the serial readout the frequency should be about 1 GHz while the maximum tested till now is 100 MHz. Therefore, the parallel solution is mandatory. The DEMAS[3] readout system [6] has shown that the Medipix parallel bus works properly up to 66 MHz and recently, preliminary results on the PRIAM[4] system [8] have proved the parallel bus at 100 MHz. For our design, we planned to clock the chip at 40 MHz frequency.

Regarding the optical link, the DAQ design started from a general purpose solution developed for high-energy physics experiments, which will be described later. With a similar approach we solved the problem of the PC interface using a digital acquisition PCI custom board already developed and tested for the MPRS[5] readout system [4].

Regarding the frame rate constraint of the DAQ design, three components play a special role in data throughput considerations: the *PCI card*, the optical link and the Medipix2 parallel bus. As mentioned before, the parallel bus features up to 400 Mbyte/s transfer rate at 100 MHz clock, the optical link can reach a throughput equal to 200 Mbyte/s while the PCI card [7] can achieve up to 90 Mbyte/s data rate. In principle, the last component represents a bottleneck for our system if its throughput is compared with the specification (>115 Mbyte/s). This problem can be overcome by splitting the readout operation in two phases: the raw data are first moved from the Medipix2 chips into a temporary storage memory and then these data are moved to the PC main memory. After the first phase, the detector can start a new acquisition while at the same time the second phase can be accomplished. Because the acquisition time is almost 36 ms long (90% of the frame period), the minimum throughput to the optical link plus PCI card chain is 12 Mbyte/s, which is much lower than the maximim PCI card data rate. As a future improvement, we could take advantage of a PCI Express card while keeping the DAQ system unchanged.

3.2. Architecture overview

The overall DAQ system (Fig. 1a) consists of four electronic cards which will be briefly described below. Two cards (Chipboard_4C and Motherboard) form the detector stage, the third (Opt-Hub) acts as the optical link interface, while the remaining one (PCI9054) is the PC acquisition board. Detector and PC are linked by an optical fibre channel. The layout scheme adopted by all readout systems developed for the Medipix2 chip till now consists of a simple chip carrier board and one separate interface card that houses all the electronic components. This solution allows optimization of the two cards separately and is more flexible if there is a need to change the sensor (semiconductor type or thickness) or to replace faulty chips. We also chose a similar solution, with a small card Chipboard_4C card containing the receptor plus some active components as we will explain below, and a separate Motherboard card containing other electronics for the detector and the optical link interface modules.

3.3. The optical link

We chose to use an optical fibre channel to link the detector to the host PC. The main advantage of this is that optical fibre offers good signal integrity over long-distance connections (several tens of metres). Moreover, the optical

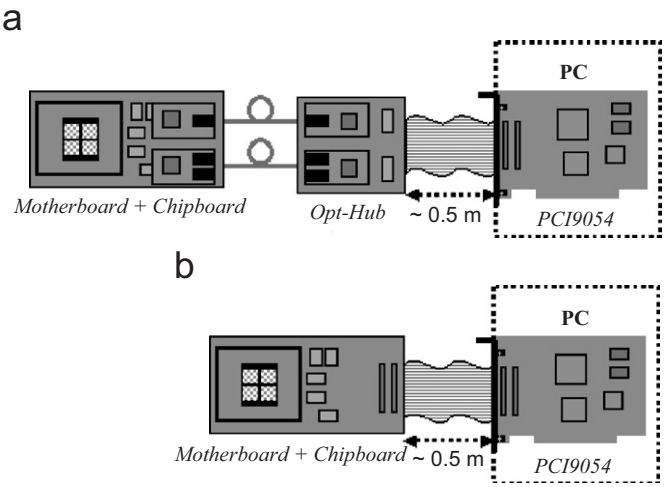

Fig. 1. PPC DAQ block diagram: (a) final setup and (b) test setup.

[2]CMOS stands for Complementary Metal Oxide Semiconductor.
[3]DEMAS stands for Dear-Mama Acquisition System.
[4]PRIAM stands for Parallel Readout Image Acquisition for Medipix.
[5]MPRS stands for Medipix Parallel Readout System.

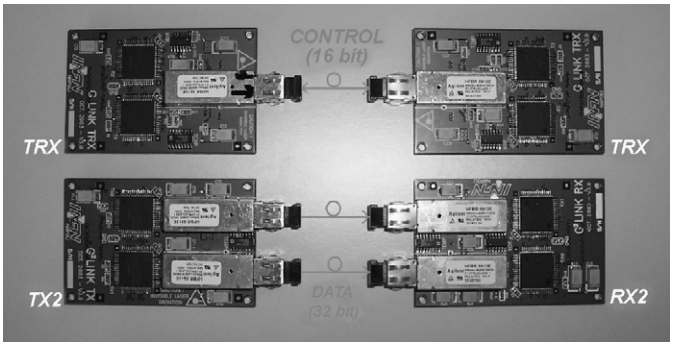

Fig. 2. Optical link stage.

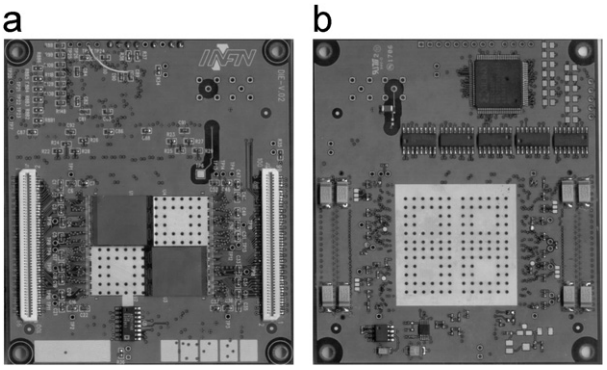

Fig. 3. *Chipboard_4C* top (a) and bottom (b) sides.

fibre is lighter than copper cables, resulting in a more compact link due to the possibility of serializing a parallel data bus into a single fibre. Such a connection is useful in the CT application, where the detector has to rotate around the sample, and allows long distance monitoring of the X-ray facility far from the X-ray tube or radioactive sources. As a drawback, the optical link option is more expensive and requires special components and additional effort in the design, development and debug phases.

The optical link stage we use is based on three different cards: a 32-bit transmitter (*TX2*) and receiver (*RX2*) and a 16-bit transmitter/receiver (*TRX*). Each $5 \times 8\,\mathrm{cm}^2$ optical module houses a Glink serializer/deserializer (HDMP-103xA) and a 805 nm VCSEL[6] laser module (HFBR-5912E). A multimode fibre is used to connect the laser modules, allowing a connection up to 100 m with a throughput of 1.28 Gbit/s on the data channel. For our project, a "RX2"/"TX2" pair is used to implement a simplex 32-bit channel for readout data while a "TRX"/"TRX" pair sets up a half-duplex 16-bit channel for configuration data, control and status signals (Fig. 2).

This modular approach shows a good level of flexibilty because it permits easy changing of the card in case of damage or its replacement with an improved version without any hardware change in the acquisition chain. On the other hand, the impossibility of integrating two optical modules in the PCI card has required the development of an additional *Opt-Hub* board.

3.4. The chipboard_4C card

The chip carrier board was specifically developed for this project: it houses one Medipix2 quad featuring the parallel bus interconnection (Fig. 3).

The presence of four Medipix2 chips and the parallel readout implementation mode implied several design constraints. First of all, the readout bus is shared by the four chips so the acquisition data have to be read sequentially. At the same time, the chips cannot be connected in daisy chain because the clock delay due to the propagation time through each chip (~7 ns) would produce, expecially for the fourth, a clock-to-data delay of the same order as the clock period (25 ns at 40 MHz).

The link with the *Motherboard* card is obtained by two slow-profile high-density 100-pin connectors. About half of the contacts are grounded and most of the remainder are for the parallel bus and power supply. Therefore, in order to limit the number of interface connections, a complex programmable logic device (CPLD) was foreseen. This directly manages all the configuration, data and clock signals of the four chips. Moreover, a 4-channel 10-bit DAC provides a variable voltage reference to each Medipix2 and one 4-channel 12-bit ADC can read the analog reference settings of the chips. Both ADC and DAC present an I2C standard interface. A voltage reference circuit is implemented for the Medipix2 internal DAC bias, while five 4-channel LVDS/CMOS tranceivers provide the appropriate signal conversion for the clock, enable and data lines of each chip.

3.5. The motherboard card

The *Motherboard* board supports the *Chipboard_4C* card and one of the optical link ends. It houses the TX2/TRX optical modules, a 4-Mbit depth FIFO[7] and one FPGA[8] which provides the Medipix2 logical interface and manages the I2C bus and the FIFO memory. Readout data coming from the Medipix2 quad are not handled by the FPGA but simply stored in FIFO memory.

The development of this card was split in two steps: first, a card without the optical link support (referred to as *Motherboard_Test)* was built, directly interfacing the PCI card through flat cables (Fig. 1a). In the second step, the board project will be modified, by adding the optical link modules. This solution simplifies the DAQ debugging and the test procedures on the *Chipboard_4C* card.

3.6. The opt-hub card

The *Opt-Hub* implements an optical link node through two optical modules: one *TRX* for the control and

[6]VCSEL stands for Vertical Cavity Surface Emitting Laser Diode.

[7]FIFO stands for First Input First Output.

[8]FPGA stands for Field Programmable Gate Array.

configuration data path and one *RX2* for incoming readout data. Each channel is buffered by dedicated FIFO memories and one FPGA manages the optical modules and FIFO's control/status signals. A double flat cable connection is provided for the *PCI9054* card link.

3.7. The PCI9054 card

The *PCI9054* card is a custom data acquisition board. It interfaces the detector stage to the PC through the standard 32 bit/33 MHz PCI bus. This board achieves a transfer rate of up to 90 Mbyte/s with direct memory access (DMA). A more detailed description about this card can be found in Ref. [7].

4. Preliminary tests

At present, the test setup (Fig. 1a) is composed of three pieces: the *PCI9054* card, the *Chipboard_4C* card with two single Medipix2 chips (without a sensor layer) on and the *Motherboard_Test* card linked to the PCI card by two 25 cm length flat cables (Fig. 4). We tested the firmware written for the *Motherboard* FPGA checking the I/O signals with an oscilloscope and logic analyzer.

After the *Chipboard_4C* CPLD programming, the whole test setup was investigated. A dedicated sofware package was written in the Microsoft Visual Basic programming language in order to manage all the operations required. To date, the following operations are implemented and tested on the FPGA/CPLD codes and tested: global chip and matrix reset, internal DAC setting (Fig. 5) and readback via external tester probing, test of the chip shift register (Fig. 6), setting of all configuration/operation bits. The procedure for matrix parameters setting is under development. The parallel readout procedure was partially tested: the logical and electrical consistency of the procedure was verified but with the actual setup only noise images can be acquired. Other chipboards bonded with 300- and 700-μm-thick silicon sensors will be available soon, allowing a complete image acquisition test.

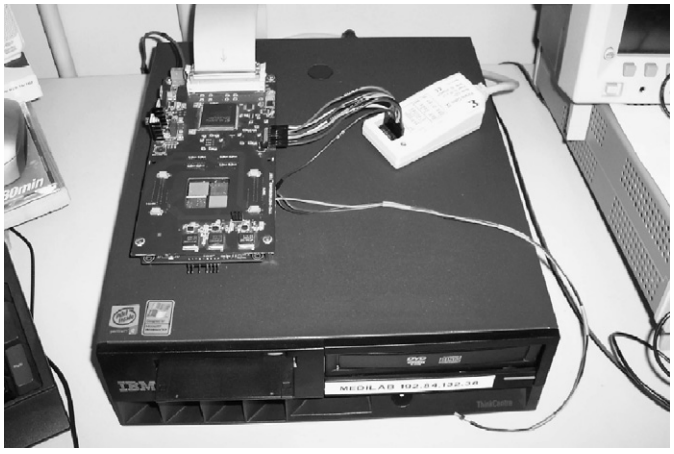

Fig. 4. Hardware test setup.

5. Conclusions

We are developing a readout system based on the Medipix2 quad detector suitable for small animal tomography applications. It exploits the Medipix2 parallel readout mode and a fast optical link to reach a data rate up to 25 frame/s. At present, a simplified version of the system with the detector stage linked to the PC by flat cables instead of optical fibre is under test, with good results. The optical link stage will be added to the readout system in a second step. The flexibility and EMI immunity offered by the optical link will make this readout system suitable for a wide range of applications when fast data acquisition rate and long-distance connections are required.

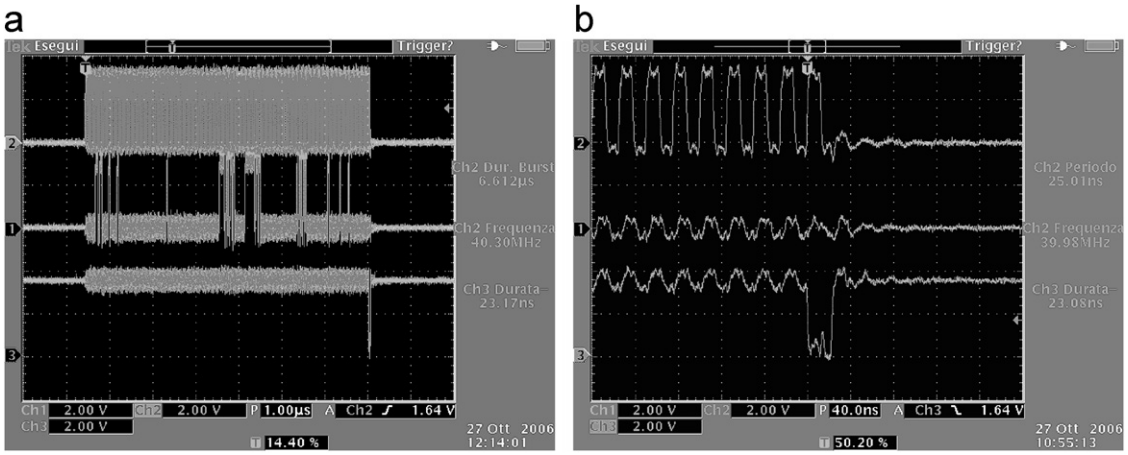

Fig. 5. (a) For the Medipix2 internal DACs settings (*SetDACs* procedure), a 256-bit coded stream is sent to the Medipix2 input serial line *DATA_IN* (middle trace). When the configuration data are loaded, the *ENABLE_OUT* signal (lower trace) goes down indicating the end of operation; (b) a zoom of the last clocks shows the ENABLE_OUT low pulse. This procedure takes 6.6 ms (256 + 8 clock cycles) at 40 MHz clock frequency.

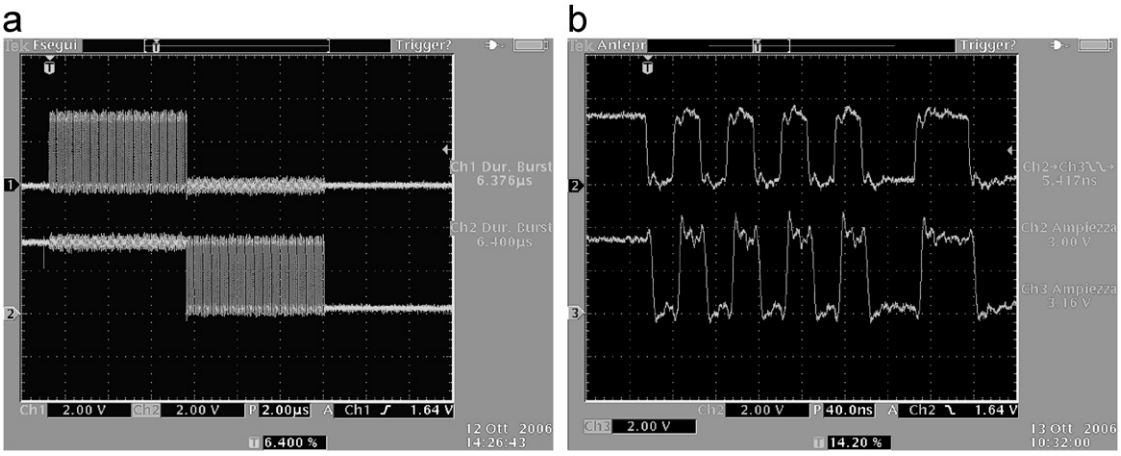

Fig. 6. (a) For the Medipix2 Fast Shift Register (*TestFSR* procedure) a 256-bit stream (upper trace) is sent to the Medipix2 serial input *DATA_IN* line. Data move through the shift register and after 256 clock cycles exit from the output *DATA_OUT* line (lower trace). If the input stream matches the output one it means that the Medipix FSR is working fine; (b) a graphical comparison between input (upper trace) and output data (lower trace) when a 256-bit delay shift register is added to the input data line. The data stream is made of a $0 \times AA$–$0 \times CC$ pattern.

Acknowledgements

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